PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

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Application No.: New U.S. Patent Application

Filed: March 30, 2001 Docket No.: 108842

For: DATA TRANSFER DEVICE AND PRINTING APPARATUS INCLUDING THE SAME

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace paragraphs **[0033] and [0036] - [0039]** as follows:

[0033] When the system clock generating circuit 40 in FIG. 2 supplies a 48 MHz system clock (see FIG. 3) to the system clock input part 5, a system clock cycle becomes $1/(48 \times 10^6)$ seconds. The system clock is input to the transfer clock circuit 6 and the clock terminals 13b, 14b, 15b, 16b of the flip-flop 13, 14, 15, 16, respectively, as described above. The transfer clock circuit 6 performs 1/10 frequency division for the system clock, to generate the pre-delayed clock. The pre-delayed clock (see FIG. 2) with a cycle of $1/(48 \times 10^5)$ seconds are output from the output part 6b of the transfer clock circuit 6.

[0036] As shown in FIGS. 2 and 3, when the HIGH level of the pre-delayed clock is input to the input terminal 13a of the flip-flop 13 from the transfer clock circuit 6, the HIGH level of the delayed clock 0 is output from the output terminal 13c of the flip-flop 13, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. As the pre-delayed clock input to the input terminal 13a becomes the LOW level, the LOW level of the delayed clock 0 is output from the output terminal 13c, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. The delayed clock 0 is delayed for one pulse of the system clock, with respect to the pre-delayed clock.

[0037] As shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 0 is input to the input terminal 14a of the flip-flop 14 from the output terminal 13c of the flip-flop 13, the HIGH level of the delayed clock 1 is output from the output terminal 14c of the flip-flop 14, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. As the pre-delayed clock 0 input to the input terminal 14a becomes the LOW level, the LOW level of the delayed clock 1 is output from the output terminal 14c, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. The timing when the delayed clock 1 makes a transition to the HIGH level or to the LOW level is delayed for one pulse of the system clock, with respect to the delayed clock 0, and is delayed for two pulses of the system clock, with respect to the pre-delayed clock.

[0038] Also, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 1 is input to the input terminal 15a of the flip-flop 15 from the output terminal 14c of the flip-

flop 14, the HIGH level of the delayed clock 2 is output from the output terminal 15c of the flip-flop 15, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. As the pre-delayed clock 1 input to the input terminal 15a becomes the LOW level, the LOW level of the delayed clock 2 is output from the output terminal 15c, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. The timing when the delayed clock 2 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 1, and is delayed for three pulses of the system clock, with respect to the pre-delayed clock.

[0039] Similarly, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 2 is input to the input terminal 16a of the flip-flop 16 from the output terminal 16c of the flip-flop 15, the HIGH level of the delayed clock 3 is output from the output terminal 16c of the flip-flop 16, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. As the pre-delayed clock 2 input to the input terminal 16a becomes the LOW level, the LOW level of the delayed clock 3 is output from the output terminal 16c, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. The timing when the delayed clock 3 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 2, and is delayed for four pulses of the system clock, with respect to the pre-delayed clock.

REMARKS

Claim 1-17 are pending. By this amendment, the Specification is amended. No new matter is introduced.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. 1.121(b)(iii)).

This application is placed in condition for initial examination. Prompt examination and allowance in due course are respectfully solicited.

Respectfully submitted,

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Attachment:
Appendix

Date: March 30, 2001

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

The following are marked-up versions of the amended paragraphs:

[0033] When the system clock generating circuit 40 in FIG. 2 supplies a 48 MHz ~~clock system~~ system clock (see FIG. 3) to the system clock input part 5, a system clock cycle becomes $1/(48 \times 10^6)$ seconds. The system clock is input to the transfer clock circuit 6 and the clock terminals 13b, 14b, 15b, 16b of the flip-flop 13, 14, 15, 16, respectively, as described above. The transfer clock circuit 6 performs 1/10 frequency division for the system clock, to generate the pre-delayed clock. The pre-delayed clock (see FIG. 2) with a cycle of $1/(48 \times 10^5)$ seconds are output from the output part 6b of the transfer clock circuit 6.

[0036] As shown in FIGS. 2 and 3, when the HIGH level of the pre-delayed clock is input to the input terminal 13a of the flip-flop 13 from the transfer clock circuit 6, the HIGH level of the delayed clock 0 is output from the output terminal 13c of the flip-flop 13, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. As the pre-delayed clock input to the input terminal 13a becomes the LOW level, the LOW level of the ~~pre-delayed clock~~ delayed clock 0 is output from the output terminal 13c, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. The delayed clock 0 is delayed for one pulse of the system clock, with respect to the pre-delayed clock.

[0037] As shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 0 is input to the input terminal 14a of the flip-flop 14 from the output terminal 13c of the flip-flop 13, the HIGH level of the delayed clock 1 is output from the output terminal 14c of the

flip-flop 14, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. As the pre-delayed clock 0 input to the input terminal 14a becomes the LOW level, the LOW level of the ~~pre-delayed clock~~ delayed clock 1 is output from the output terminal 14c, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. The timing when the delayed clock 1 makes a transition to the HIGH level or to the LOW level is delayed for one pulse of the system clock, with respect to the delayed clock 0, and is delayed for two pulses of the system clock, with respect to the pre-delayed clock.

[0038] Also, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 1 is input to the input terminal 15a of the flip-flop 15 from the output terminal 14c of the flip-flop 14, the HIGH level of the delayed clock 2 is output from the output terminal 15c of the flip-flop 15, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. As the pre-delayed clock 1 input to the input terminal 15a becomes the LOW level, the LOW level of the ~~pre-delayed clock~~ delayed clock 2 is output from the output terminal 15c, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. The timing when the delayed clock 2 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 1, and is delayed for three pulses of the system clock, with respect to the pre-delayed clock.

[0039] Similarly, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 2 is input to the input terminal 16a of the flip-flop 16 from the output terminal 16c of the flip-flop 15, the HIGH level of the delayed clock 3 is output from the output terminal 16c

of the flip-flop 16, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. As the pre-delayed clock 2 input to the input terminal 16a becomes the LOW level, the LOW level of the ~~pre-delayed clock~~ delayed clock 3 is output from the output terminal 16c, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. The timing when the delayed clock 3 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 2, and is delayed for four pulses of the system clock, with respect to the pre-delayed clock.